## REMARKS

Claims 1-8 are in the application. Claims 1-8 are being amended. No amendment is made to the drawings. No new matter is added.

The drawings are objected to under 37 CFK 1.83(a) as not showing every feature of the invention specified in the claims. The recitation "continuous-time sigma-delta conversion means" is deleted from the claims and replaced by 'continuous-time sigma-delta modulator'. Figures 1 and 2 of the drawings show examples of continuous-time sigma-delta modulators as stated at page 3 lines 14-17 and page 4 lines 4-5 and lines 26-27, for example.

Claims 1-8 are rejected under *35* U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the Examiner objects that "it is not clear in what drawing the circuit of claim 1 reads on." In the case of claim 1, it is submitted that an example of the sigma-delta modulator appears in Fig. 1 and again in Fig. 2 and examples of the delay module (previously referred to a s delay means) appears in Fig. 5 and again in Figs, 7, 8 and 9. Therefore it is respectfully submitted that the requirement for the claim elements to be illustrated in the drawings is met.

Similarly, it is submitted that all the elements of claims 5 to 8 are shown correctly in the drawings.

Regarding claim 3, the elements recited can be found in the example of Fig. 9 as follows:

- first series of delay elements: 16
- further series of delay elements: 27
- adjustment element: 25, 26, 24, 28
- said train of primary clock pulses: claim 1 line 5

Claim 2 has been amended to provide a clear antecedent basis for 'first series of ... delay elements'. The recitation "said further series" in claim 3 at line 4 has its antecedent in line 2 of claim 3.

Claim 3 has been amended to clarify the 'adjustment element', which generates an adjustment signal $V_{TUNE}$ by comparison between the primary signal (CLK) and the

output of the 'further series' of delay elements 27 in the phase detector 25, filtered in the filter 26. This adjustment signal $V_{TUNE}$ is applied over a feedback loop to the bias circuit 24 of the further series of delay elements 27, correcting the delay of the further series, and the same adjustment signal $V_{TUNE}$ is then applied to make the same correction to the first series of delay elements 16. It is therefore submitted that, at least as amended, claim 3 is clear and is not indefinite.

Accordingly, it is submitted that claims 1 to 8 are allowable. Issue of a patent on this application is requested.

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action since reasons for the patentability of each pending claim are provided without addressing these statements. Therefore, Applicants reserve the right to address these statements at a later time if necessary.

No amendment made herein is related to the statutory requirements of patentability unless expressly stated herein. Further, no amendment herein is made for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

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